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(54) **Demodulation of an IF-signal by a sigma-delta converter.**

(57) A sigma-delta signal converter is implemented using switched capacitor switching elements in which a first switch (31) serves as a mixer (11). The output of the mixer is directed to the second input of an adder (16), and its second input is the feedback signal (f1) of the sigma-delta signal converter, which is also directed into a base-frequency output signal through a decimator (14) and low-pass filtering (15).

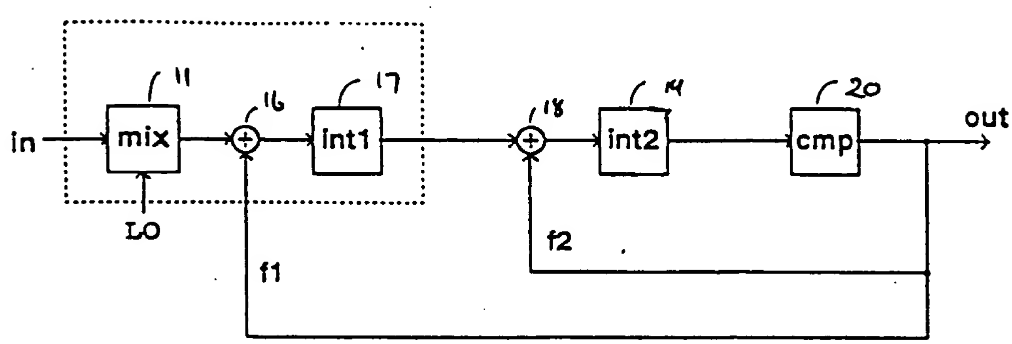

Fig. 3

EP 0 643 477 A2

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The invention relates to a receive arrangement for receiving a modulated carrier signal.

EP 0 461 720-A1 describes a known receive arrangement for receiving a modulated carrier signal, comprising a mixer/demodulator driven with a sinusoidal oscillator of carrier frequency fc, at least one adder, a low-pass filter, a pulse shaper constituting a one-bit sigma-delta signal converter, all included in a closed signal loop, the pulse shaper being driven with sampling frequency fs, and further comprising a digital decimation filter. In this type of receive arrangement the modulated carrier signal is demodulated in the closed signal loop by the mixer/demodulator, the output signal of which is converted after passing through the low-pass filter into a digital signal by the sigma-delta converter.

A typical prior art sigma-delta converter arrangement is described in greater detail with reference to Figure 1 of the drawings.

An incoming intermediate frequency IF carrier signal is provided to each branch of the receive arrangement. In each branch the incoming signal is filtered through bandpass filter 1 and mixed to a baseband signal in a linear mixer 2 using a sinusoidal local oscillator signal LO1 at the IF frequency. A high time constant capacitor 3 is provided on each of the incoming signal branches to remove direct currents from the baseband signal. The gain of the circuit is controlled through Automatic Gain Controllers (AGC) 5 and the baseband signals are converted to digital signals in modulators 6. After modulation the signals pass through respective decimators 7 and post filters 8 to remove spurious signals created by the decimators. The specific details of the local oscillator frequency and phase shifts of the particular arrangement illustrated in Figure 1 are as follows:

$$\mathrm{PHI1} = +45°$$
$$\mathrm{PHI2} = -45°$$
$$\mathrm{PHI3} = \mathrm{PHI4} = 0°$$
$$\mathrm{LO1} = \mathrm{IF}$$
$$\mathrm{LO2} = \text{oversampling frequency}$$

The demodulation, i.e., the mixing of the intermediate frequency (bandpass-filtered) int-signal down to the base frequency is traditionally based on the use of a multiplier. Thus the modulated IF-signal is multiplied by the sinusoidal oscillator signal (LO1). In the synchronous demodulation the frequency and the phase of the oscillator are locked to the carrier wave with the aid of a phase-locked loop (PLL), for instance. The frequency spectrum of the mixed product consists of the desired base-frequency component and the component spectrums which are removed by low-pass filtering prior to entering the sigma-delta converter. Such a mixing process may be described by the following trigonometric equation:

$$\cos(a) * \cos(b) = 1/2 * \cos(a - b) + 1/2 * \cos(a + b) \quad (1)$$

Equation (1) holds only if both products are pure cosine signals.

If cos(a) now represents the modulated int-carrier wave then:

$$a = \omega 0 * t + \mathrm{PHI}, \quad (2)$$

where ω0 is the angle frequency of the carrier wave and PHI is a momentary phase modulation (QAM, MSK, QPSK, GMSK, ...).

Ideally the term cos(b) represents a clean, mixing oscillator frequency (LO):

$$b = n * \omega 1 * t \qquad (n = 1,2,3, ...) \quad (3)$$

where n*ω1 is the angular frequency of the oscillator of the mixer.

In the ideal case the frequency and the phase of the oscillator are locked to the frequency and the phase of the carrier wave of the input signal (in). In these conditions ω0 = n*ω1, and the term 1/2*cos(a-b) is reduced to 1/2*cos(PHI). This base-frequency phase difference signal conveys the data symbols. Term 1/2*cos(a+b) represents the component of the frequency spectrum on frequency 2*ω0.

When prior art receive arrangements such as those described above are implemented by discrete components they require a very large area on the printed circuit board. In addition, as the signal entering the sigma-delta converter is a baseband signal the ac-coupled branches need very high high-pass corner frequencies with high time constants in order to accomplish dc blocking. This means that it is not efficient for the arrangement to be powered down as often as would be ideal, as powering up again is slow and as a result the circuit cannot be powered down for short periods. The circuit therefore, consumes a large amount of power.

In accordance with the present invention there is provided a receiver for receiving a modulated carrier signal comprising, a sigma-delta signal converter having at least one adder included in a feedback loop, characterised in that the arrangement comprises a time discrete sampling means for down converting the modulated carrier signal prior to the feedback loop.

By down converting the carrier frequency signal using a time discrete sampling means a number of advantages are provided. Firstly, an expensive sinusoidal oscillator is no longer required with space and cost benefits. Secondly, although use of time discrete sampling means, rather than a pure sinusoidal local oscillator for down converting the IF signal means that mixing occurs at the frequency of sampling and also at harmonics of the sampling frequency this perceived disadvantage can be used to the system's advantage enabling samples to be taken using a local oscillator sampling at a subharmonic frequency of the carrier signal. Thus can also give important power savings.

One way in which the invention can be implemented is by using the input stage of a sigma-delta signal converter having switched capacitor switching

elements to implement the time discrete sampling means that acts as a mixer. The sigma-delta converter with the desired switched capacitor switching elements provided at the input stage may as an ASIC. The output of this mixer can then be directed to the first input of an adder included in the closed feedback signal loop of the sigma-delta converter. This adder comprises, as the second input, the feedback signal of the sigma-delta signal converter, which is also directed through a decimator and low-pass filter to provide an output signal which is provided to the second input of the adder.

In circuits of embodiments of the invention the incoming modulated signal may be mixed into a base-band frequency signal or a frequency approaching the base-band frequency prior to entering the closed feedback loop.

Sigma-delta converters are traditionally used in converting base-band signals. However, in accordance with to the invention, they can now be adapted for converting intermediate frequency signals directly.

Difficult ac-coupling problems, control and high-pass filtering problems are solved by circuit arrangements of embodiments of the invention. Similarly, power consumption can be decreased by shortening the time for switching the receiver on from stand-by to the active state. This enables the circuit to be powered down when not in use for shorter periods than would conventionally be possible as a capacitance with a lower time constant is adequate for dc blocking.

An additional advantage can be gained by using switched capacitors to provide some of the automatic gain control of the circuit. This means that the number of AGC-circuits required by the receive arrangement as a whole can be decreased. With embodiments of the invention part of the necessary filtering can also be provided without the need for additional filters between the mixing and a-d converting stages by utilising a digital filter already present in the sigma-delta converter.

Embodiments of the invention can be utilized advantageously in, for example, radio telephones.

Embodiments of the invention will now be described in greater detail with reference to Figures 2 to 4 of the drawings of which:

Figure 2 is a block diagram of a sigma-delta converter included in a receive arrangement according to one embodiment of the invention;

Figure 3 is a schematic representation of a switched capacitor switching element suitable for implementing the mixing and automatic gain control functions of the embodiment of Figure 2; and

Figure 4 is a schematic representation of an embodiment of a receive arrangement including the sigma-delta converter of Figure 2 operating with a local oscillator at or near the carrier frequency of the incoming signal.

The receive arrangement of an embodiment of the invention is illustrated in Figure 2 using a sigma-delta analog-digital converter with a large dynamic input range in which a mixer 11 is implemented using switched capacitor switching elements 30-39 illustrated in Figure 4. The switched capacitor switching elements providing the mixing function of the mixer 11 are driven by a square wave local oscillator signal (LO1) at (or near) the frequency of the IF signal. Both the mixer and the local oscillator signal are digital. Switched capacitor switching elements are also provided to implement an automatic gain controller (AGC) 12 providing an automatic gain control function for the circuit. The receive arrangement includes a bandpass filter 10, and each branch further includes a modulator 13 that converts signals from analog signals to digital signals, a decimator 14 and a post filter 15 which perform the same functions as the correspondingly named portions of the prior art receive arrangement illustrated in Figure 1. The prefiltering of the signal (after modulation) can be designed to freely correspond to the design demands of the respective circuit and the dc-deviation of the sigma-delta converter can be corrected using the internal, digital correction of deviations.

The phase and frequency details for the local oscillator signals provided to the respective branches are as follows:

$$PHI3 = +45°$$
$$PHI4 = -45°$$
$$LO1 = IF$$

A base-frequency output signal is obtained from the modulator after the decimator and the low-pass filter which can be processed to retrieve the modulating information. Because the signal entering the sigma-delta converter arrangement is an IF signal, only a short time-constant capacitor 9 is necessary for preventing dc signals from transferring to the sigma-delta converter. This means that the device can be powered up and down more quickly and as less power is required to power up, short term power downs are practical making the arrangement more power efficient than conventional receive arrangements.

The mixer 11, AGC 12 and modulator 13 are described in greater detail with reference to Figure 3. The modulated reception signal (in), for instance a bandpass-filtered int-signal from the RF-part of the radio telephone, is directed to the mixer 11 (mix) to which the local oscillator (LO1) signal is also applied. LO1 may be on or around the carrier frequency of the received signal (in) or a subharmonic of that frequency. The output of mixer 11 is directed to a first adder 16, the second input of which is a feedback signal f1. The output of the first adder 16 is directed to an integrator 17. The output of the integrator 17 is directed to a second adder 18, the second input of which is a feedback signal f2. The output of the second adder 18 is directed to a second integrator 19 and further to a

comparator 20. The output signal (out) of the comparator 20 is further directed to the decimator 14 the (low-pass) post filter 15 for filtering out unwanted signals resulting from mixing of LO1 and the carrier signal.

The output signal provides a base-frequency signal which can be processed using digital signal processing means, for instance. The output signal (out) is coupled to the first and second adders (f1) and 18 (f2) in respective feedback branches.

The second adder 18, the second integrator 19 (int2) and the comparator 20 (cmp) provide a second closed feedback loop in the circuit. Those skilled in the art know the basic idea of the sigma-delta converter, therefore it is not described in more detail in this connection. More detailed discussion can be found in the articles: The Design of Sigma-Delta Modulation Analog-to-Digital Converters, Bernhard E. Boser, Bruce A. Wooley, IEEE Journal of Solid-State Circuits, Vol. 23 No.6 December 1988 and Oversampling Delta-Sigma Data Converters, Theory, Design and Simulation J.C. Candy and G.C. Temes IEEE press 1992 both incorporated herein by reference.

Typically in the prior art an analogue bandpass filter is provided prior to entering the modulation stage of the sigma-delta converter to remove unwanted signals resulting from mixing. In the present case, however, the digital filtering function of the sigma-delta converter itself can be used to remove the unwanted signals.

Figure 4 shows the input stage of the receive arrangement of the embodiment of Figure 2 showing switched capacitor switching elements of the mixer 11 and the AGC 12 in greater detail. A first capacitor 30 is used to sample and hold the incoming signal. First switches 31, 32 are closed to provide a sample to the first capacitor 30. Once the input signal has been sampled, a third switch 33 is closed to transfer the charge on the first capacitor 30 to the output. Second and third (and possibly further) capacitors 34, 35 are provided in parallel with the first capacitor 30. These are each controllably connected to the input and output through a pair of switches 36, 37; 38, 39. By closing the appropriate switches and adding parallel capacitance from one or more of the second and third capacitors 34, 35 the signal transfer ratio can be changed. The switches are under the control of an external cpu and can be used to replace automatic gain control steps of the circuit as a whole. In this way amplification steps can be included in the sigma-delta modulator by altering the ratios of the input capacitancies.

The mixer 11 can be considered as a sample and a hold circuit that samples the input signal in synchronization with the oscillator and directs the samples to the output as a signal which remains constant for the period of the sampling interval. The oscillator signal (LO) is therefore represented by a square wave with a base frequency of $n^*\omega 1$. Instead of the term $\cos(b) = \cos(n^*\omega 1^*t)$ of equation (1), the following series of odd harmonics is obtained:

$$\cos(n * \omega 1 * t) + 1/3 * \cos(3 * n * \omega 1 * t) + 1/5 * \cos(5 * n * \omega 1 * t) + \ldots \quad (4)$$

The cosine terms of a higher order are mixed in the mixer (1) with the input signal (in) producing sum and difference components of the frequencies to the spectrum of the output signal of the mixer (1). All input signals on a higher frequency than the base frequency are filtered by a filter before entering the mixing stage of the sigma-delta converter.

It is preferable to use the first switch 1 of the switched capacitor switching element as the mixing element. In this case, signal bands around the multiples of the frequency of the local oscillator signal LO are folded onto the base frequency. The local oscillator base frequency or its subharmonics can therefore be used to down convert the carrier signal to the base-band or a frequency approaching the base-band. The unwanted signals resulting from mixing using the local oscillator are removed by filtering.

Referring back to Fig. 2, the inventive idea is realized in the circuit arrangement of this embodiment of the invention in accordance with which switched capacitor switching elements present in the input stage of a sigma-delta converter are used to implement the mixer 11 which directly demodulates the IF-signal into a base-frequency signal; in other words, the IF-signal and its multiples are folded on the base frequency. The first switch 31 in the input of stage of the sigma-delta converter is utilized here to serve as the mixer 11.

The embodiment of Figures 2 to 4 can be implemented using a local oscillator having a frequency LO1 that is the same as or approaching the frequency of the IF carrier signal. Although it would generally be desirable for LO1 to have the same frequency as the incoming signal it may in many instances be desirable or merely practical to use a local oscillator frequency LO1 offset slightly from the frequency of the IF carrier signal. The mixing frequency could, for instance, be LO + Δf (where LO is the frequency of the IF carrier). In this case the signal (in) applied to the input is folded to the frequency Δf which is almost to the baseband frequency. If the modulated intermediate frequency (in) is 1010 kHz, the mixing signal LO + Δf may be 900 kHz, for instance, whereby the demodulated signal is on the frequency of -110 kHz with respect to the base-band frequency.

One example of when it may be practical to use a local oscillator with a frequency slightly offset from the IF carrier frequency is when a driver conveniently located in the sigma-delta converter for providing a square wave local oscillator for driving the mixer 11 does not coincide exactly with the IF carrier signal. Another example is when it is desirable to provide four times oversampling. Under these circumstances the

subsequent digital mixer can be implemented more easily when the signals are at a frequency Δf offset from the baseband. Typically a signal within 1 MHz of the carrier frequency is acceptable for down converting the incoming signal.

In a conventional arrangement, if the mixing frequency of a sinusoidal local oscillator differs from the IF carrier signal by Δf, the term cos(b) of equation (1) is solved by the following formula:

$$b = n * \omega_1 * t + \Delta\omega * t, \quad (5)$$

where $\Delta\omega$ is the angular frequency corresponding to frequency Δf.

Although equation (1) deals with the mathematics of the prior art solution using a sinusoidal local oscillator, once the down converted signal generated by mixing using the time discrete sampler of embodiments of the present invention is filtered prior to entering the a-d modulation stage, it is effectively a pure cosine signal and equation (1) holds.

The receive arrangement of Figures 2 to 4 can also be used to down convert the incoming signal to the baseband (or a frequency approaching the baseband) using a subharmonic of the carrier frequency. In these circumstances the phase and frequency details for the local oscillator signals provided to the respective branches are as follows:

$$PHI3 = +45/N°$$
$$PHI4 = -45/N°$$
$$LO1 = IF/N$$

In other respects the arrangement operates in the same manner as previously described.

When the input signal (in) is branched into two different branches, it is possible to arrange the receive circuit arrangements of embodiments of this invention in each of the branches. The demodulation of an I/Q-modulated signal (I = in the phase, Q = in the phase shift of 90 degrees) may be implemented simply in this way using principles known per se and described by way of example in Digital Communication, Edward A. Lee, David G. Messershmitt, Kluwer Academic Publishers, Boston, 1990 incorporated herein by reference. The clocks of the modulators of both branches are synchronized.

Those skilled in the art will notice that the circuit arrangements of embodiments of the invention are simple to implement using relatively few circuit elements. They result in decreased power consumption and accelerated operation of the circuit (fast shifting from the stand-by state to the active operating state and vice versa) which is especially significant for radio telephones.

The present invention includes any novel feature or combination of features disclosed herein either explicitly or any generalisation thereof irrespective of whether or not it relates to the claimed invention or mitigates any or all of the problems addressed.

In view of the foregoing description it will be evident to a person skilled in the art that various modifications may be made within the scope of the invention.

Claims

1. A receiver for receiving a modulated carrier signal comprising, a sigma-delta signal converter having at least one adder included in a feedback loop, characterised in that the arrangement comprises a time discrete sampling means for down converting the modulated carrier signal prior to the feedback loop.

2. An electronic receive arrangement according to claim 1 wherein the time discrete sampling structure comprises a switching member under the control of a square wave signal.

3. An electronic receive arrangement according to claim 2 wherein the frequency of the square wave signal is the carrier signal frequency or a subharmonic of the carrier signal frequency.

4. An electronic receive arrangement according to claim 2 wherein the frequency of the square wave frequency is selected so that the frequency of the down converted signal is intermediate the carrier frequency and the frequency of the baseband signal.

5. An electronic receive arrangement according to any preceding claim wherein the time discrete sampling means comprises switched capacitor switching elements.

6. An electronic receive arrangement for receiving a modulated carrier signal, the arrangement comprising a sigma-delta signal converter, a mixer/demodulator controlled on the carrier frequency or its subharmonic frequency or on a frequency at least close to these, and at least one adder included in a closed signal loop, characterized in that the received, modulated carrier signal (in) is first directed to the input stage (10) of the sigma-delta signal converter which is implemented as a time discrete sampling structure, the first member (1) of which serves as the mixer, that the output of the mixer is directed to the first second input of said adder (3) and that the second input (f1) of the adder (3) is the feedback signal (out) of the sigma-delta signal converter, whereby the output signal (out) is directed into a base-frequency output signal through a decimator and low-pass filtering.

7. A receive arrangement according to claim 6, characterized in that the mixing member (1) is essen-

tially a switching member which is directed by a square wave signal on the carrier frequency (LO) or on its subharmonic (LO/n) frequency, whereby the signal (in) applied to the input is folded on the base frequency.

8. A receive arrangement according to claim 6 or 7, characterized in that the mixing frequency (LO) is replaced by frequency LO + Δf, whereby the signal (in) applied to the input is folded on a nearly base-frequency intermediate frequency Δf.

9. A receive arrangement according to claims 6, 7 or 8, characterized in that said input stage (10) is implemented using components of a switched capacitor integrator.

10. A receive arrangement according to any preceding claim characterized in that the sigma-delta converter comprises at least one adjustable amplification step for automatic gain control (AGC).

11. An IQ-mixer/demodulator in which the input signal is divided into two branches I (in phase) and Q (quadrature), respectively, characterized in that the receive arrangement according to any of the preceding claims is used in both branches.

12. A receive arrangement according to claim 11, characterized in that the required phasing arrangement is either made for the input signal (in), the local one (LO), or for both of them.

13. The utilization of the receive arrangement according to any of the preceding claims in a radio telephone.

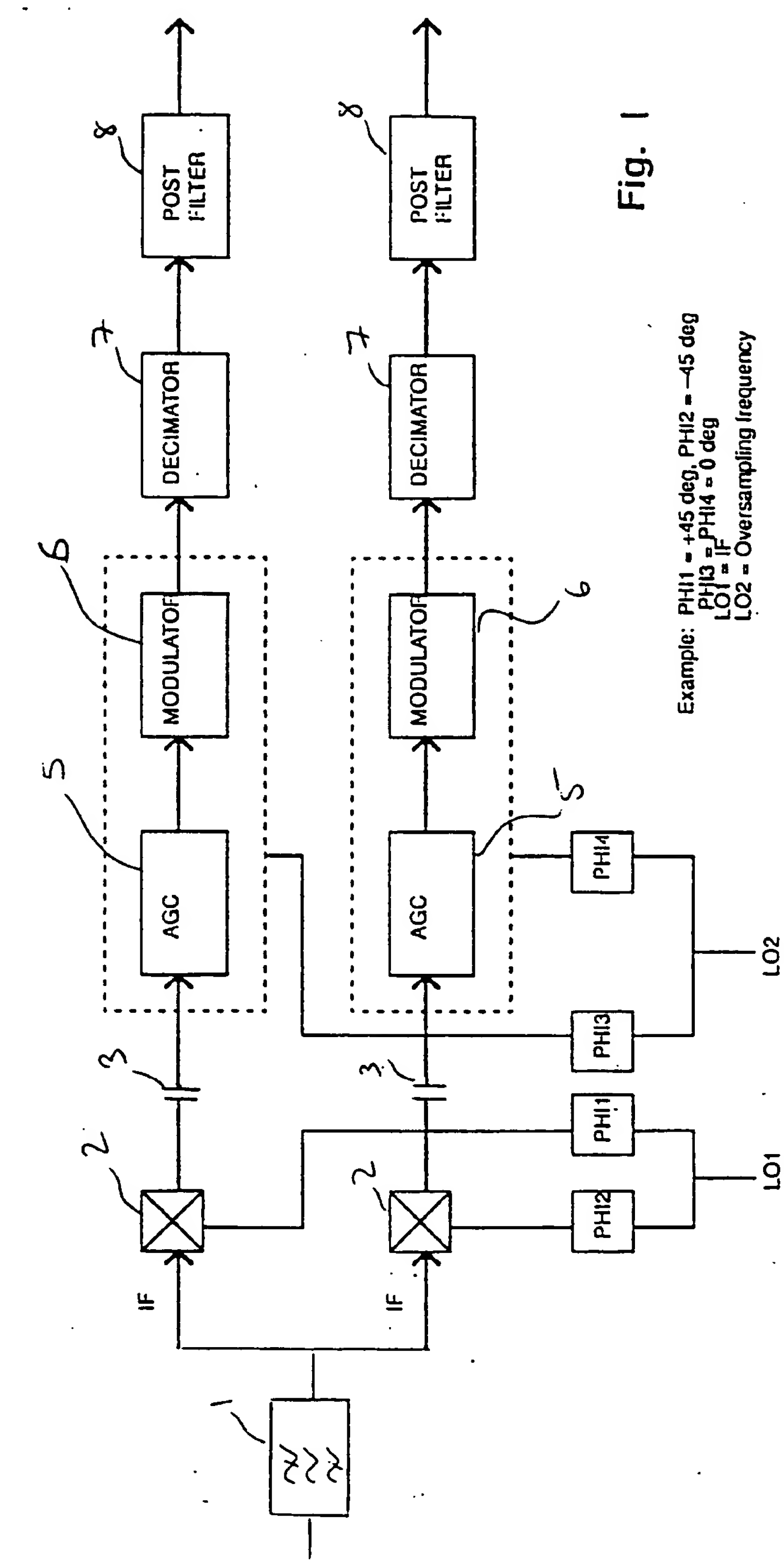
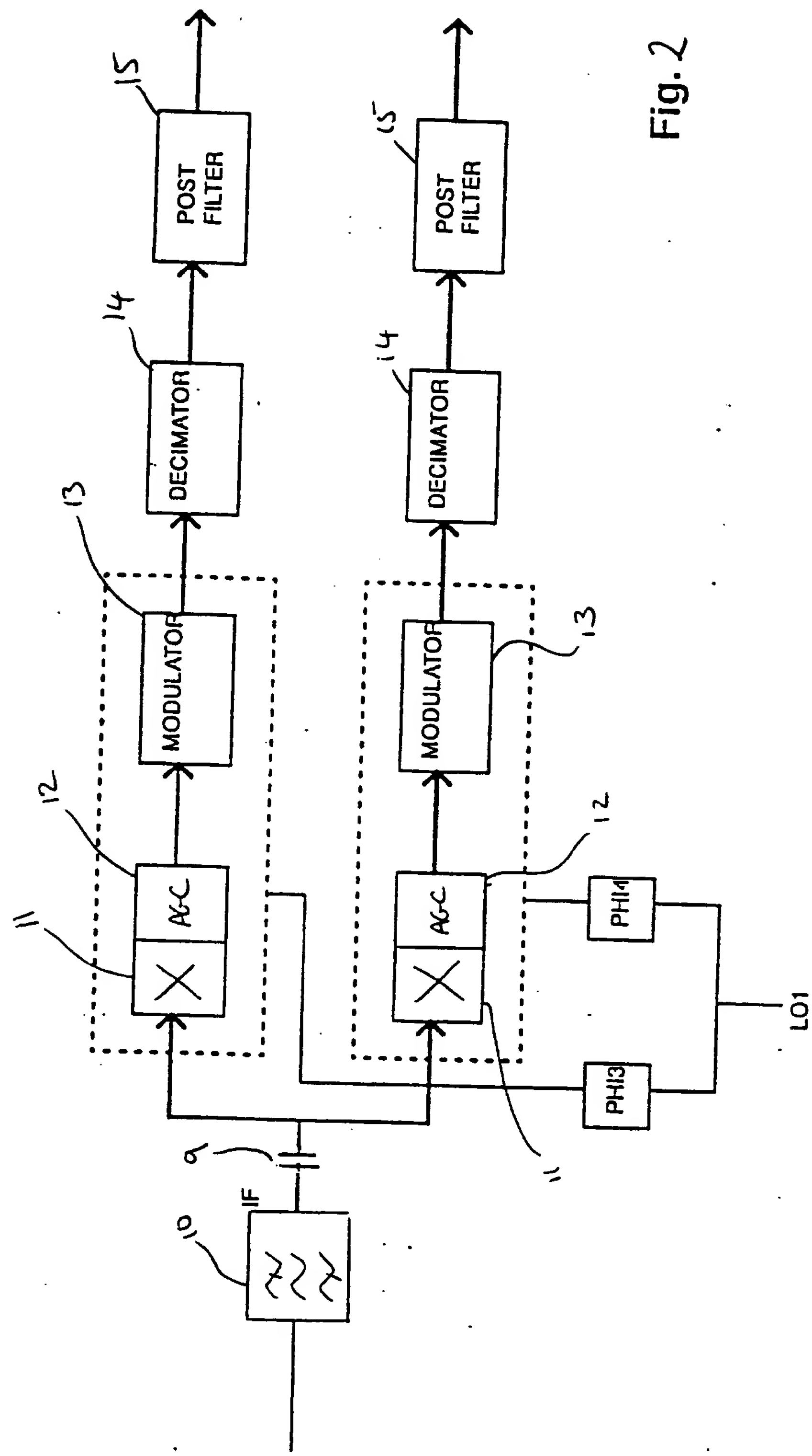

IF
IF
AGC
MODULATOR
DECIMATOR
POST FILTER
PHI1
PHI2
PHI3
PHI4
LO1
LO2
Example: PHI1 = +45 deg, PHI2 = −45 deg
PHI3 = PHI4 = 0 deg
LO1 = IF
LO2 = Oversampling frequency

Fig. 1


POST FILTER
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PHI4
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9
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Fig. 2

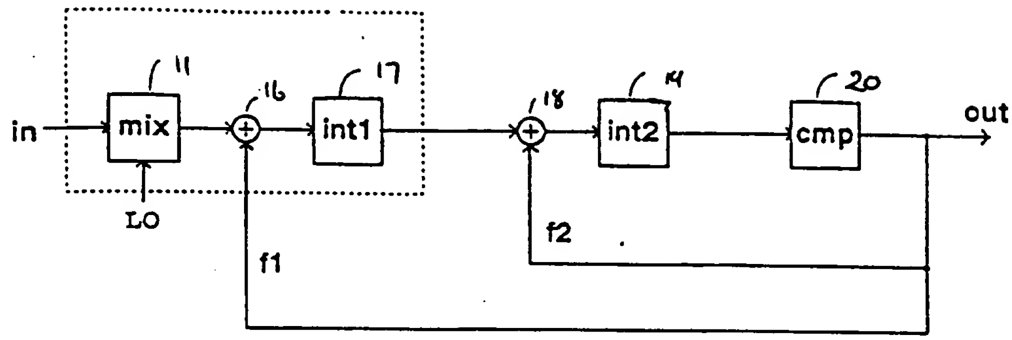
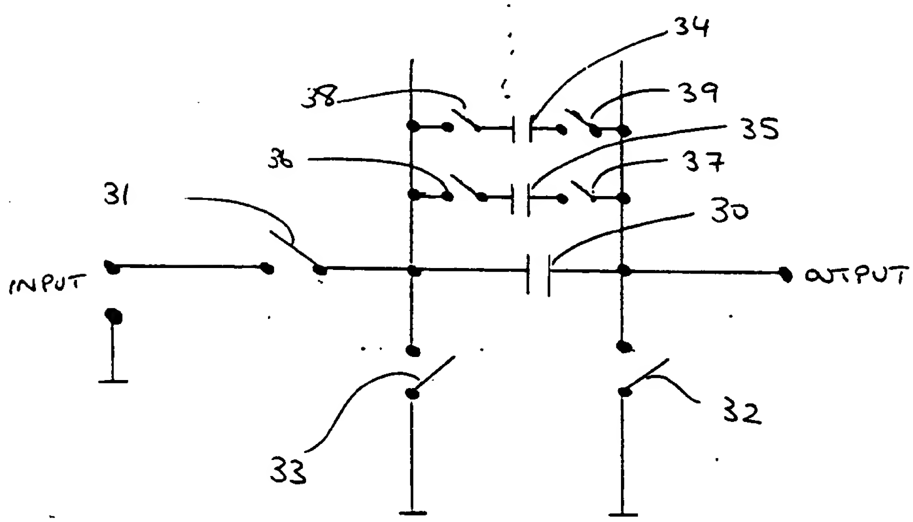

in
mix
11
LO
16
int1
17
f1
18
int2
14
cmp
20
out
f2

Fig. 3


34
38
39
35
36
37
31
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INPUT
OUTPUT
33
32

FIG4